CLAIMS:

1. A power limiter comprising input terminals and a transmission line arranged to couple a high frequency signal supplied to the input terminals to an output of the power limiter, the transmission line comprising a plurality of successive transmission line sections, each transmission line section comprising at least a series inductance and a shunt capacitance, the shunt capacitance comprising a capacitance of at least two oppositely poled diodes connected in parallel to an output of the respective transmission line section to limit voltage of said signal at said output of the respective transmission line section, wherein at least two of the transmission line sections have different numbers, decreasing from said input terminals towards said output of the power limiter, of diodes connected in series with one another and constituting each of said at least two oppositely poled diodes of the respective transmission line sections.

2. A limiter as claimed in claim 1 wherein said diodes connected in series with one another comprise an array of a plurality of parallel-connected sets of diodes, each set comprising a plurality of diodes connected in series.

3. A limiter as claimed in claim 1 wherein each diode comprises a MESFET having a source and drain connected together.

4. An integrated circuit device comprising a limiter as claimed in claim 1 and a high frequency circuit having an input coupled to the output of the limiter.

5. An integrated circuit device as claimed in claim 4 wherein the high frequency circuit comprises an amplifier.

6. An integrated circuit device as claimed in claim 4 wherein the device comprises a gallium arsenide integrated circuit device.

7. A high frequency signal power limiter comprising a plurality of transmission line sections connected in succession, each transmission line section comprising:

two input connections;

two output connections;

at least one inductance coupling the two input connections to the two output connections; and

at least two oppositely-poled diodes coupled in parallel between the two output connections to limit voltage of said signal between said output connections;

wherein each of said at least two oppositely poled diodes of at least each of the successive transmission line sections except a last one of the successive transmission line sections comprises a plurality of diodes connected in series, a number of said plurality of diodes connected in series decreasing for the successive transmission line sections towards said last one of the successive transmission line sections, whereby the successive transmission line sections limit said signal to successively decreasing voltages.

8. A limiter as claimed in claim 7 wherein said plurality of diodes connected in series comprise an array of a plurality of parallel-connected sets of diodes, each set comprising a plurality of diodes connected in series.

9. A limiter as claimed in claim 7 wherein each diode comprises a MESFET having a source and drain connected together.

10. A gallium arsenide integrated circuit comprising a limiter as claimed in claim 7 and a high frequency circuit having an input coupled to an output of the limiter.

11. A limiter for limiting a high frequency signal, comprising a plurality of transmission line sections connected in succession, each transmission line section comprising at least one series inductance coupling an input to an output of the transmission line section, and two oppositely-poled parallel-connected shunt diode arrays coupled at the output of the transmission line section to limit voltage of said signal at said output;

wherein the diode arrays comprise different numbers of diodes, connected in series, with the number of series diodes of the arrays decreasing progressively for the plurality of transmission line sections from an input of the limiter to an output of the limiter.

12. A limiter as claimed in claim 11 wherein the diode arrays further comprise a plurality of diodes connected in parallel.

13. A limiter as claimed in claim 11 wherein each diode array comprises a square array of diodes.

14. A limiter as claimed in claim 11 wherein each diode comprises a MESFET having a source and drain connected together.

15. A gallium arsenide integrated circuit comprising a limiter as claimed in claim 11 and a high frequency circuit having an input coupled to an output of the limiter.